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Transmitter and Translating Receiver Design For 64-ary Pulse Position Modulation (PPM)

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ABSTRACT

This paper explores the architecture and design of an optically-implemented 64-ary PPM transmitter and direct-translating receiver that effectively translates incoming electrically-generated bit streams into optical PPM symbols (and vice-versa) at > 1 Gb/s data rates. The PPM transmitter is a cascade of optical switches operating at the frame rate. A corresponding receiver design is more difficult to architect and implement, since increasing data rates lead to correspondingly shorter decision times (slot times and frame times). We describe a solution in the form of a time-to-space mapping arrayed receiver that performs a translating algorithm represented as a code map. The technique for generating the code map is described, and the implementation of the receiver as a planar lightwave circuit is given. The techniques for implementing the transmitter and receiver can be generalized for any case of M -ary PPM.

Keywords: Modulation, pulse-position-modulation, M -ary PPM, planar lightwave circuits (PLCs), photonic integrated circuits (PICs), direct translating receiver

1. INTRODUCTION

M -ary pulse position modulation (M -ary PPM) signaling is a means of transmitting multiple bits per symbol in an intensity modulated/direct detection (IM/DD) system¹. PPM is used in applications with average power limitations. In optical communication systems, PPM becomes challenging to implement at high rates and/or large M using electrical processing, since the PPM time slots and frame (decision) times become increasingly small, as shown in Figures 1 and 2. The figure covers the range $M=2, 4, 8, \dots, 256$ and data rates of 10 Mb/s to 40 Gb/s. For slot times falling below 25 ps, the electronic bandwidth requirements of the sampling and decision times become restrictive; therefore, photonic signal processing should be investigated.

We have been exploring techniques for PPM transmission and receiving using optical processing. Previous work² described a transmitter system architecture that directly translates an electrically-generated bit sequence of N bits into an M -ary optical PPM symbol for any $M=2^N$. It has been considerably more difficult to define a similar receiver algorithm that directly translates the received optical pulse position directly back to a bit sequence with minimal electronic processing. Designs for $M=4$ based on virtual array receivers have been shown and implemented,³ but were considered difficult to scale to larger M ^{2,4}. More recently, we described the foundations for a generalized direct translating receiver, with an $M=16$ example⁵. In this

work, we present a generalized code construction technique for the PPM translating receiver that is applicable to all M and data rates and show the designs for an $M=64$ PPM system.

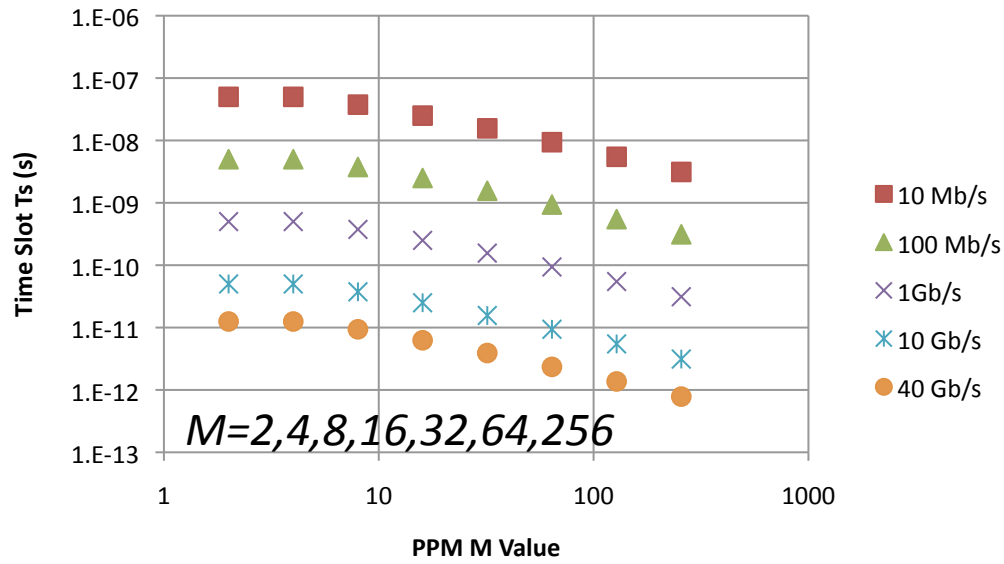


Figure 1. Time Slot T_s (s) as a Joint Function of Data Rate and M -ary Value (not including guard time or line coding).

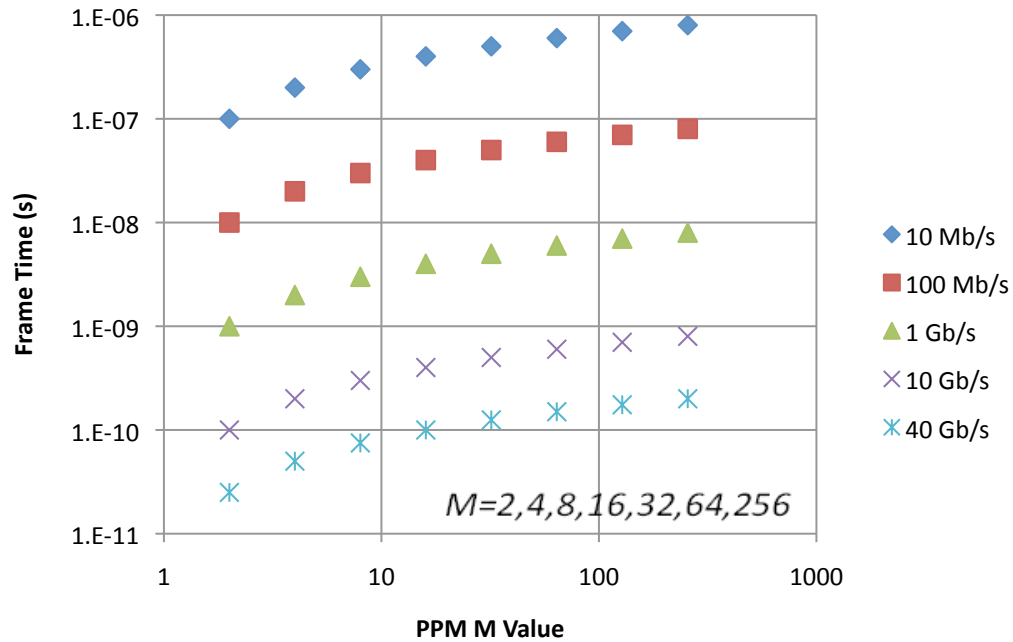


Figure 2. Frame Time (s) as a Joint Function of Data Rate and M -ary Value (not including guard time or line coding).

2. TECHNICAL DISCUSSION

The PPM transmitter/receiver system architecture we have been exploring is based on a PPM symbol represented in the time domain as a series of contiguous frames. Each frame is divided into M slots of width T_s , and the placement of a pulse (with width $< T_s$) into the m th slot uniquely identifies the symbol. In binary format, m represents one of $M = 2^N$ values within the set $S = \{0, 1, 2, \dots, m, \dots, M-2, M-1\}$ and can be expressed as

$$m = b_{N-1}2^{N-1} + b_{N-2}2^{N-2} + \dots + b_n2^n + b_22^2 + b_12^1 + b_02^0$$

$$= \sum_{n=0}^{N-1} b_n 2^n$$

where b_n is the binary value (0 or 1) of the corresponding bit within the sequence of N bits.

2.1. PPM Transmitter System Architecture

The PPM transmitter pulse encodes an optical carrier into a PPM symbol based on incoming binary data. The specific design for $M=64$ is shown in Fig. 3, but can be generalized for any M . The transmitter accepts an optical carrier consisting of a pulse train that repeats at the frame rate. It is sent through a cascade of N 1x2 optical switches whose paths are recombined. Each path applies a different delay to the pulse, and the accumulated delays shift the carrier pulse into the m th slot. The amount of unit shift applied by each switch is $(2^n \times b_n)$, as controlled by the n th bit of the data sequence. In Fig. 3, the switches are implemented as dual output Mach-Zehnder interferometers (MZI) modulators. The bit sequence is demultiplexed using D-flip flops controlled by a divided, staggered clock operating at the frame rate.

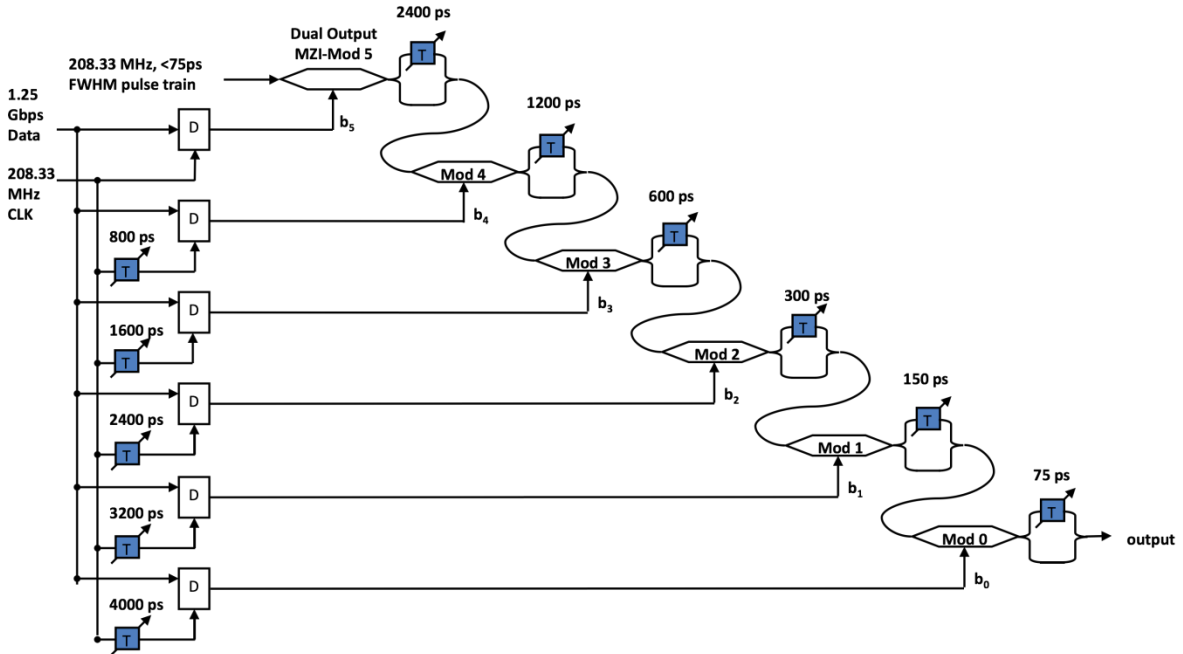


Figure 3. Architecture of the 64-ary PPM Encoder at 1.25 Gb/s (corresponding to 1 Gb/s data with 8B/10 line coding and no guard time).

At 1.25 Gb/s (1 Gb/s with 8B/10B line coding), six $[N=\log_2(64)]$ such modulator/delay line pairs are required for the implementation with PPM frame times of 4.8 ns and slot times of 75 ps. Each modulator is driven by the bits of the demultiplexed input bit sequence at a rate of 208.33 MHz, and each parallel delay line can apply a delay of $2^i \times 75$ ps. The required input pulse train for the encoder must have pulse widths of <75 ps (to fit within the slots) and a repetition rate of 208.33 MHz (to correspond to the frame rate).

2.2. PPM Receiver System Architecture

In generalized PPM receiver systems, the determination of the transmitted symbol is performed using a comparison test of the M possible slots, where a decision is made based on which slot contains the most energy (i.e. contains the pulse). The logical structure of the PPM direct translating receiver thus performs this comparison test while simultaneously producing the binary representation of the transmitted symbol. The operation can be represented as a form of map coding, consisting of an $N \times M$ array of cells where, as before, $N=\log_2 M$. The code sets for 4-ary and 8-ary PPM are given in Figures 4 and 5. The M columns represent the slot positions of a transmitted frame, where an asterisk denotes the presence of unit pulse energy within a slot, identifying the PPM symbol. The N rows represent the bits b_n outputted by the receiver as the binary translation. The receiver compares the slots by sampling the slots simultaneously at the frame rate. This is done optically by copying the incoming frame and aligning the slots to the receiver sample window. The amount of delay applied to each slot is denoted in the code as $s_n = n \times T_s$ in Figure 4 and can be applied similarly for the codes of other M . Simultaneously with the comparison test, the receiver performs translation of the received slot to its binary representation, as determined by the shading of each cell. The map is colored in the following way: in the top row the first half ($M/2$ of the cells) is shaded, the second half is unshaded; in the second row the cells are grouped into $M/4$ subarrays, with group one and three shaded and group two and four unshaded; this is continued to the N th row which is divided into M cells, with the odd cells shaded and the even cells unshaded. The summation of energy in the unshaded cells subtracted by the energy in the shaded cells across each row will then produce a positive or negative value that can be respectively associated as a binary “1” or “0”.

Having demonstrated the map coding as a means of defining the PPM direct translating receiver, we depict the coding map and the directly related receiver architecture for $M=64$. The coding map is shown in Figure 6 and the derived receiver implementation is shown in Figure 7. Copies of the incoming frame are generated using optical splitters, creating a copy for each cell of the code. The copies are also respectively delayed by s_n . Combiners group the aligned slots of the frame together into the rows of the code map, additionally grouping them according to their color along each row. The slots that are associated with unshaded cells forward to the positive input of a balanced photodetector while slots of shaded cells go to the negative input. The balanced photodetectors then effectively performs the subtraction of the shaded cells from the unshaded cells. By setting the receiver threshold to zero, the correct bit is produced. The sampling window of the receiver should be of duration T_s synchronized at the frame rate. Depending on M and the data rate, this sampling could be done electronically or with an optical time gate. If implemented using optical gating, the bandwidth requirements of the balanced photodetector and any subsequent electronics can be relaxed to operate at the frame rate rather than the slot rate. As M and data rate increase, the implementation of the receiver as a planar lightwave circuit (PLC) becomes necessary in order to attain the precise delays required to align the slots. More

importantly, erbium doped waveguide amplifiers (EDWAs) can also be integrated into the PLC design in order to compensate for insertion losses incurred by splitting and combining⁶.

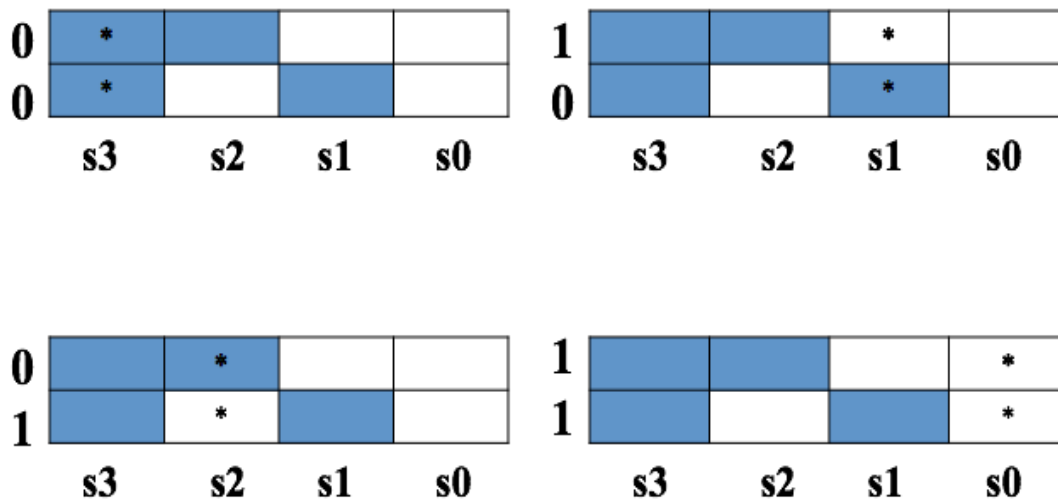


Figure 4. Coding Map for 4-ary PPM Showing Unique Association of PPM Alphabets and Map Columns.

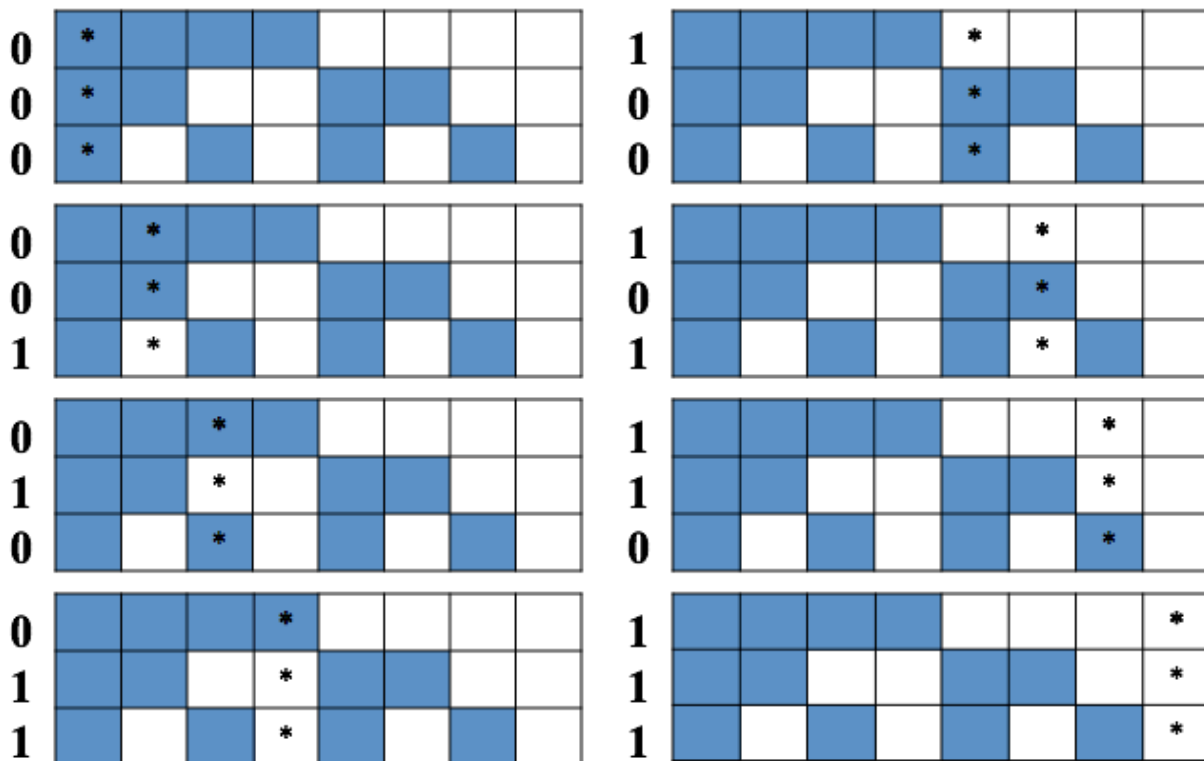


Figure 5. Coding Map for 8-ary PPM Showing Unique Association of PPM Alphabets and Map Columns.

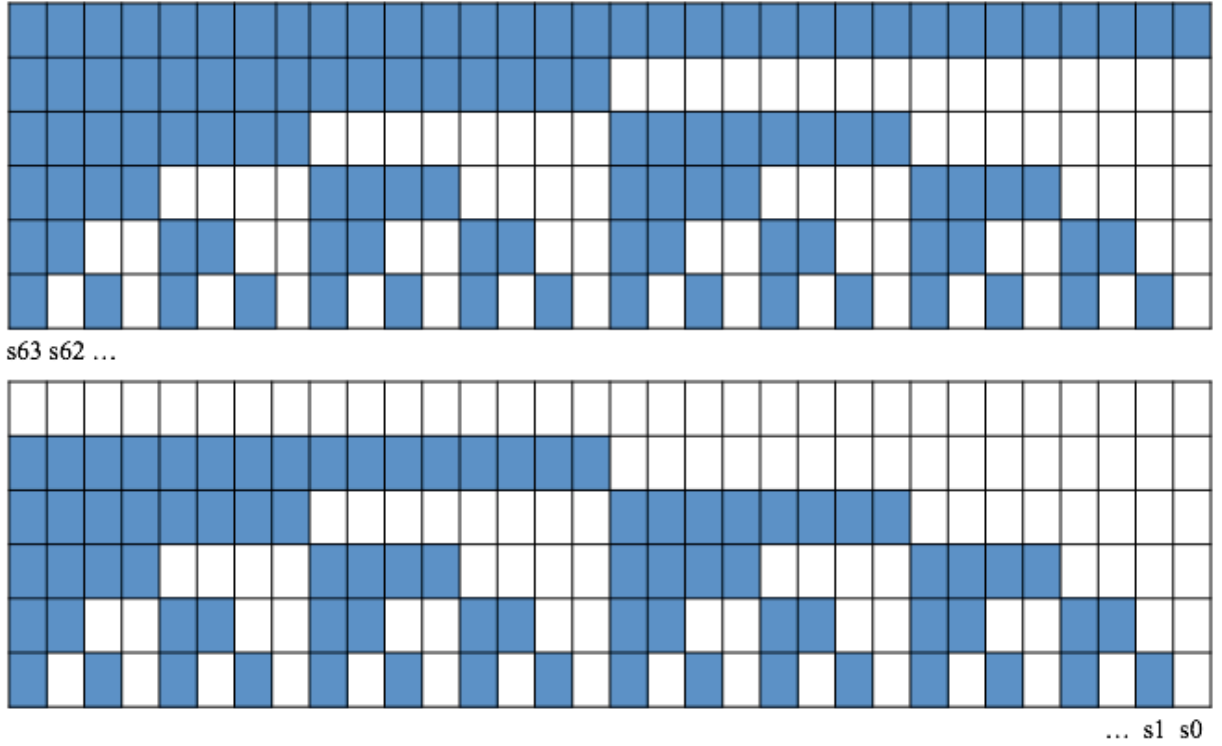


Figure 6. Coding Map for 64-ary PPM Showing Unique Association of PPM Alphabets and Map Columns.

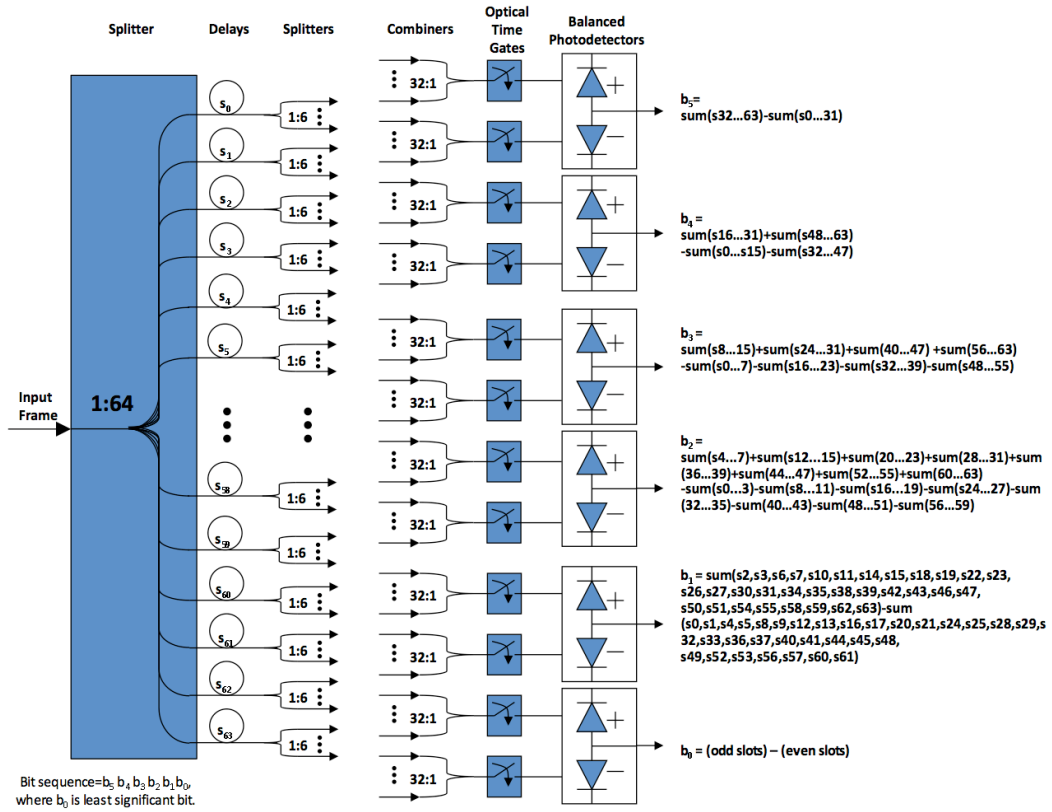


Figure 7. System Architecture of the 64-ary Direct Translating Receiver.

3. CONCLUDING REMARKS

We have described technique for architecting PPM transmitters and direct translating receivers for all M and data rates. The receiver directly identifies the PPM encoded bit sequence with optical processing and relaxes electronic bandwidth requirements after photodetection. The receiver can be represented as a coding map, and the equivalent physical implementation has been presented for the case of $M=64$ and 1 Gb/s using a planar lightwave circuit.

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